What is claimed is:

1. A Flash memory device comprising:

a control circuit;

a memory array with a plurality of floating gate memory cells arranged in a plurality of erase blocks, wherein each erase block of the plurality of erase blocks contains 128 sectors, and each sector contains a user data section of 512 bytes;

an erase block management data structure formed into a control data section of a first six sectors of each erase block of the plurality of erase blocks, wherein each control data section of the first six sectors contains a 6 byte erase block management data field; and

a plurality of RAM control registers.

2. The Flash memory device of claim 1, wherein a first 3 bytes of the 6 byte erase block management data field contain an erase block management data and a second 3 bytes of the 6 byte erase block management data field contain a 1s complement converted copy of the erase block management data of the first 3 bytes.

3. The Flash memory device of claim 1, wherein the first six sectors of each erase block of the plurality of erase blocks are arranged into 3 groups of 2 sector pairs, wherein both sectors of each 2 sector pair contains a complete copy of a erase block management data stored in the 2 sector pair.

4. A Flash memory device comprising:

a memory array containing a plurality of floating gate memory cells arranged in a plurality of erase blocks; and

an erase block management data structure arranged in each erase block of the plurality of erase blocks.

5. The Flash memory device of claim 4, wherein each of the plurality of erase blocks is further arranged into a plurality of sectors.

6. The Flash memory device of claim 4, wherein the erase block management data structure is configured in a fault tolerant data structure.

7. The Flash memory device of claim 6, wherein the fault tolerant data structure is an erase block management data field and a 1s complement copy of the erase block management data field.

8. The Flash memory device of claim 6, wherein the fault tolerant data structure is a copy in a second sector of the erase block of an erase block management data field contained in a first sector of the erase block.

9. A Flash memory device comprising:

a memory array containing a plurality of floating gate memory cells divided into a plurality of erase blocks, wherein each of the plurality of erase blocks is further divided into a plurality of sectors; and

an erase block management data structure arranged in each erase block of the plurality of erase blocks.

10. The Flash memory device of claim 9, wherein each sector of the plurality of sectors has a user data section and a control data section.

11. The Flash memory device of claim 10, wherein the control data section has an erase block management data field.

12. The Flash memory device of claim 11, wherein the erase block management data field is a six byte data field.

13. The Flash memory device of claim 9, wherein a first set of sectors of the plurality of sectors contain erase block management data structures.

14. The Flash memory device of claim 13, wherein the first set of sectors of the plurality of sectors comprises a first six sectors of each erase block of the plurality of erase blocks.

15. A Flash memory device comprising:

a memory array containing a plurality of floating gate memory cells arranged in a plurality of erase blocks; and

an erase block management data structure arranged in each erase block of the plurality of erase blocks, wherein each erase block of the plurality of erase blocks has an erase block state that is recorded in the erase block management data structure of the erase block.

16. The Flash memory device of claim 15, wherein the erase block state is one of "erased", "invalid", "partially filled", or "fully valid".

17. The Flash memory device of claim 16, wherein the erase block state is allowed to transition directly from the "partially filled" state to the "invalid" state.

18. The Flash memory device of claim 15, wherein each erase block of the plurality of erase blocks contains a contiguous range of logical sector addresses.

19. The Flash memory device of claim 15, wherein each erase block of the plurality of erase blocks contains a single logical sector address that is repeated within the erase block.

20. A Flash memory device comprising:
a memory array containing a plurality of floating gate memory cells arranged in a plurality of erase blocks;
a control circuit; and
an erase block management data structure arranged in each erase block of the plurality of erase blocks.

21. The Flash memory device of claim 20, wherein the control circuit stores equivalents of the erase block management data structures of each erase block of the plurality of erase blocks into a RAM data structure.

22. The Flash memory device of claim 20, wherein the control circuit maps a logical address to a physical address of the plurality of erase blocks.

23. The Flash memory device of claim 20, wherein the control circuit manages a state of each erase block and erase block management data structure of the plurality of erase blocks.

24. The Flash memory device of claim 23, wherein the erase block management data structure of each individual erase block of the plurality of erase blocks contains erase block management data for the individual erase block.

25. The Flash memory device of claim 23, wherein each erase block and erase block management data structure of the plurality of erase blocks is written with an updated user data and an updated erase block management data with a single erase block write operation.

26. A system comprising:

a host coupled to a Flash memory device, wherein the Flash memory device comprises,

a memory array containing a plurality of floating gate memory cells arranged in a plurality of erase blocks, and

an erase block management data structure arranged in each erase block of the plurality of erase blocks.

27. The system of claim 26, wherein the Flash memory device appears to the host as a rewriteable storage device.

28. The system of claim 26, wherein the host is a processor.

29. The system of claim 26, wherein the host is a computer system.

30. The system of claim 26, wherein an interface to the Flash memory device is compatible with a mass storage device.

31. The system of claim 26, wherein an interface to the Flash memory device is a PCMCIA-ATA compatible interface.

32. A method of making a Flash memory device comprising:

forming a memory array containing a plurality of floating gate memory cells arranged in a plurality of erase blocks; and

forming an erase block management data structure in each erase block of the plurality of erase blocks.

33. A method of operating a Flash memory device comprising:
storing an erase block management data structure in each erase block of a plurality of erase blocks of a Flash memory array.

34. The method of claim 33, wherein storing the erase block management data structure further comprises storing the erase block management data structure in an at least one sector of each erase block of the plurality of erase blocks.

35. The method of claim 34, wherein storing the erase block management data structure in the at least one sector of each erase block of the plurality of erase blocks further comprises storing an erase block management data value in a control section of the at least one sector.

36. The method of claim 34, wherein storing the erase block management data structure in the at least one sector of each erase block of the plurality of erase blocks further comprises storing an erase block management data value in a 6 byte data field of the at least one sector.

37. The method of claim 33, wherein storing the erase block management data structure further comprises storing the erase block management data structure in a first set of sectors of each erase block of the plurality of erase blocks.

38. The method of claim 37, wherein storing the erase block management data structure in a first set of sectors of each erase block of the plurality of erase blocks further comprises storing the erase block management data structure in an initial 6 sectors of the erase block.

39. A method of operating a Flash memory device comprising:
storing a fault tolerant erase block management data structure in a plurality of sectors of each erase block of a plurality of erase blocks of a Flash memory array.

40. The method of claim 39, wherein storing the fault tolerant erase block management data structure in the plurality of sectors of each erase block of the plurality of erase blocks further comprises storing a component of the erase block management data structure in a first erase block management data field and a 1s complement copy of the component of the erase block management data structure in a second erase block management data field.

41. The method of claim 39, wherein storing the fault tolerant erase block management data structure in the plurality of sectors of each erase block of the plurality of erase blocks further comprises storing a copy of an erase block management data field contained in a first sector of the erase block in a second sector of the erase block.

42. A method of operating a Flash memory device comprising:
placing an erase block management data structure in at least one sector of each erase block of a plurality of erase blocks of a Flash memory array; and
recording an erase block state in the erase block management data structure in the at least one sector of each erase block of the plurality of erase blocks.

43. The method of claim 42, wherein recording the erase block state in the erase block management data structure in the at least one sector of each erase block of the plurality of erase blocks further comprises recording an erase block identifier that identifies erase block format and content in the erase block management

data structure in the at least one sector of each erase block of the plurality of erase blocks.

44. The method of claim 43, wherein recording the erase block identifier further comprises recording an erase block identifier that identifies the erase block as containing a contiguous range of logical sector addresses.

45. The method of claim 43, wherein recording the erase block identifier further comprises recording an erase block identifier that identifies the erase block as containing a single logical sector address that is repeated within the erase block.

46. The method of claim 42, wherein recording the erase block state in the erase block management data structure in the at least one sector of each erase block of the plurality of erase blocks further comprises recording the erase block state as one of "erased", "invalid", "partially filled", or "fully valid".

47. The method of claim 46, wherein recording the erase block state further comprises allowing the erase block state to transition directly from "partially filled" to "invalid".

48. The method of claim 42, wherein recording the erase block state in the erase block management data structure in the at least one sector of each erase block of the plurality of erase blocks further comprises recording the erase block state with an erase block operation that writes both a user data and the erase block management data in a single write operation.

49. The method of claim 42, further comprising storing the contents of the erase block management data structures of each erase block of the plurality of erase blocks into a RAM data structure.

50. A method of operating a Flash memory device comprising:

placing an erase block management data structure in at least one sector of each erase block of a plurality of erase blocks of a Flash memory array; and

mapping a logical address to a physical erase block and a sector address of the plurality of erase blocks.

51. The method of claim 50, wherein mapping the logical address to the physical erase block and sector address of the plurality of erase blocks further comprises managing a state of each erase block and erase block management data structure.